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SP4 and replaces AVEVA Plant 12.1.SP4.21. AVEVA Plant includes AVEVA PDMSâ„¢, AVEVA Engineeringâ„¢, AVEVA Diagramsâ„¢ and related products. - see below. AVEVA Plant is an integrated plant design and control solution designed specifically for utilities and industry. Its core capabilities include the following functional subsystems: - design (PDM, PDM/PLM, PDM/PLM/CI, PDM/PLM/CC); - production management (PLM); - object design and simulation (PDM/PDM/CI/PDM/PLM/CI); - process management (CI); - human resource management (PDM/PDM/CI/PDM/PLM/CC);

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Aveva Pdms 12.1 sp4 Aveva Pdms 12.1 sp4 Aveva Pdms 12.1 sp4.44 aveva pdms manual Aveva Pdms 12.1 SP4 52 aveva pdms manual 38 pdf Aveva PDMS 12.1 SP4 Scoring the PDMS-2 Read the Guide to Item Administration pg 1-52 and Examiner's Manual pg. Aveva PDMS - drafting module basics di Amerighi einai CADD World 4 anni fa 4 minuti e 52 secondi 2.036 visualizzazioni This Video tutorial teaches how toÂ .1. Field of the Invention The present invention relates to a semiconductor memory device and a method of manufacturing the same, more particularly, to a nonvolatile memory device using floating gate type memory cells and a method of manufacturing the same. 2. Description of the Related Art FIG. 9 illustrates a sectional view of a conventional nonvolatile memory device. The nonvolatile memory device has a well region 12 formed on a semiconductor substrate 11. The well region 12 and a well isolation region 13 are formed from a P-type well region. A source region 14 and a drain region 15 are formed in an upper portion of the well region 12. A floating gate electrode 17 is formed on the semiconductor substrate 11 with an insulating film therebetween. The floating gate electrode 17 is insulated from the semiconductor substrate 11 by an insulating film 16. A control gate electrode 18 formed on the floating gate electrode 17 via a silicon oxide film 19. A bit line 20 made of a metal is connected to the drain region 15. The well region 12 is formed by ion implantation of the P-type impurities and the well isolation region 13 is formed by ion implantation of the P-type impurities into the entire surface of the semiconductor substrate 11. The floating gate electrode 17 is insulated from the semiconductor substrate 11 by the insulating film 16. This insulating film 16 is made of, for example, silicon oxide or silicon nitride. The insulating film 16 is formed by, for example, thermally oxidizing the exposed surface of the semiconductor substrate 11 and the surface of the floating gate electrode 17. After forming the insulating film 16, polysilicon is deposited on the entire surface of the semiconductor substrate 11. Then c6a93da74d